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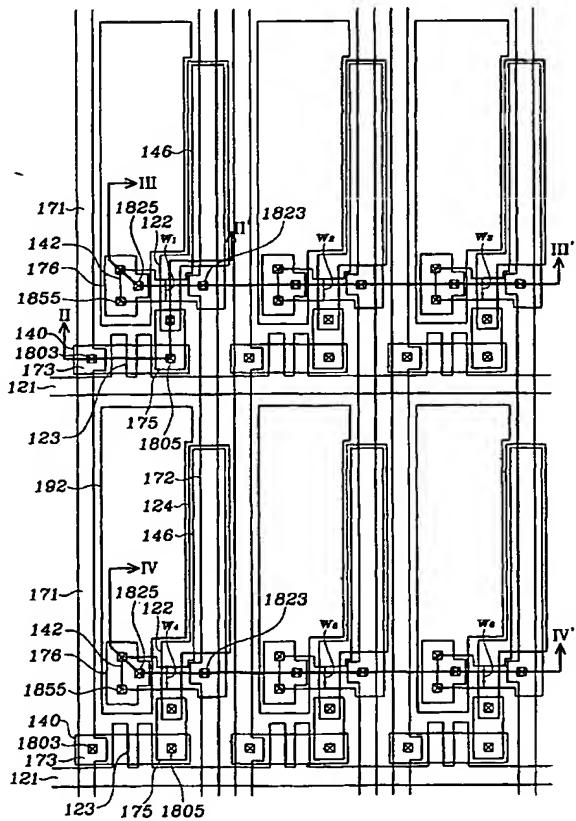
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(54) Title: THIN FILM TRANSISTOR ARRAY PANEL



(57) Abstract: A thin film transistor array panel is provided, which includes: a substrate (110) including a plurality of pixel areas; a semiconductor layer (140, 142) formed on the substrate (110) and including a plurality of pairs of first (140) and second (142) semiconductor portions in respective pixel areas; a first insulating layer (130) formed on the semiconductor layer; a gate wire (121-124) formed on the first insulating layer; a second insulating layer (180) formed on the gate wire (121-124); a data wire (171, 172) formed on the second insulating layer (180); a third insulating layer (185) formed on the data wire (171, 172) a pixel electrode (192) formed on the third insulating layer (185) and connected to the data wire (171, 172), wherein width and length of at least one of the first (140) and the second (142) semiconductor portions vary between at least two pixel areas.



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B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPODOC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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| A | US 2002063287 A1 (YAMAZAKI et al.) 30 May 2002 (30.05.2002) <i>claims 1,2.</i> | 1,4 |

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| Patent document cited in search report | Publication date | Patent family member(s) | | | Publication date |
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